An Accurate Design Algorithm for LLC Resonant Converters—Part II

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***Abstract*—This paper proposes a new approach to optimally design LLC converters. The core of the proposed approach is an accurate algorithm that can find all the possible designs satisfying the peak-gain requirement. Designers can conveniently evaluate several design results and find the optimal one for their respective applications. Part II of this paper discusses design considerations and procedure using the proposed algorithm. Case studies reveal different design tradeoffs in different application scenarios. A 384-V nominal 300-V minimum input voltage range 12-V/50-A output LLC converter prototype with 97.3% peak efficiency is built to verify the proposed design algorithm.**

***Index Terms*—LLC converter, modeling, resonant power conversion, switched-mode power supply.**

I. Introduction

LLC converter has advantages, such as zero-voltage switching, wide gain range, narrow switching frequency variation range, etc. Benefiting from its advantages and new packaging technologies, LLC converters can be highly efficient and compact [1]–[30], and are used in applications, such as telecommunication [2], LED lighting [6], [8], [9], [12]–[17], battery chargers [21], servers, and renewable energy applications [22]–[30].

Many design methods for LLC converters are based on fundamental harmonic approximation or its derived methods [31]–[43]. Existing design methods often use the peak-gain requirement and frequency-domain analysis, together with an additional restrictive condition to determine the LLC resonant tank parameters. The additional conditions include predefined dead time, operation at no-load condition, secondary-side leakage inductance, switching frequency range, short-circuit operation, etc. [30]–[32], [35]–[37], [41]. However, many restrictive conditions are rather arbitrary and unnecessary; thus, the resultant LLC converter design may not be an optimal design.

From efficiency optimization point of view, a more logical design approach is to find out all possible designs that meet the peak-gain requirement, and then select the optimal design based on loss analysis at the targeted operating condition, which varies from application to application. Part I of this paper proposed an accurate algorithm to obtain all the designs with the same peak gain at the same minimum switching frequency. In Part II, the proposed algorithm will be verified through simulation and case studies. Furthermore, it will be demonstrated that any LLC converter design can be expressed by resonant-tank characteristic impedance and turn-off current at resonant frequency, which can be further transformed into an equivalent design of any resonant frequency. The component stresses of equivalent designs are the same. Therefore, the proposed algorithm covers all possible LLC designs. Following the case studies, a design procedure is provided to guide users use the proposed algorithm.

The sections are organized as follows. Section II verifies the accuracy of the proposed algorithm, and discusses insights about component stresses, ZVS considerations, peak-gain reduction by dead time, peak-gain-dominated design, and component tolerances. Section III discusses transformation of a given design into an equivalent design with an arbitrary resonant frequency. Section IV provides a design flowchart to utilize the proposed algorithm to design LLC converters. Section V demonstrates experimental results of a prototype LLC converter designed using the proposed algorithm. Section VI concludes this paper.

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TABLE I
Specification of Design Example 1

Nominal input voltage	384 V
Minimum input voltage	280 V
Minimum input voltage with ZVS	375 V
Output voltage	12 V
Minimum switching frequency	100 kHz
Full load power	600 W
Transformer turns ratio	16 : 1

II. Algorithm Verification and Discussions

The accuracy verification of the proposed algorithm is provided in this section followed by discussions on component stress. Simulation is used here because it can accurately set component values as needed for verification purpose and avoid measurement errors. For the sake of completeness, the same verification results have been provided at the end of Part I.

A. Design Example 1: Algorithm Accuracy Verification

The design specification of a design example is summarized in Table I. The design results from the proposed algorithm are listed in Table II.

It is noted that all the design results in Table II should provide 12-V/50-A output power at 280-V input voltage and 100-kHz switching frequency. PSIM simulation software is used to verify

TABLE II
DESIGN RESULTS FROM THE PROPOSED ALGORITHM

Design No.	C_r (nF)	L_r (μH)	L_p (μH)	Resonant Frequency (kHz)
1	6	380.9244	111.7068	105.275
...	...	...	...	...
5	10	210.597	118.6049	109.6716
...	...	...	...	...
10	15	123.7436	131.1616	116.8189
...	...	...	...	...
15	20	77.9608	150.3098	127.458
...	...	...	...	...
20	25	47.0212	175.7023	146.7923
21	26	41.6328	181.3471	152.9733
22	27	36.3778	186.9216	160.5905
23	28	31.2196	192.1061	170.2266
24	29	26.152	196.3064	182.7547
25	30	21.2914	198.3318	199.1394

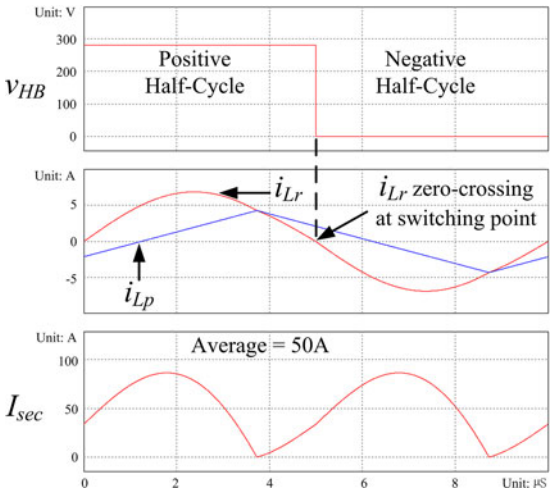

Fig. 1. Peak-gain point of Design Example 1. Design No. 1. $V_{\rm in} = 280$ V, $V_o = 12$ V, $F_s = 100$ kHz. Output current is exactly 50 A.

the design accuracy of the Design Nos. 1, 10, 20, and 25. The simulation results are shown in Figs. 1–4.

In Figs. 1–4, the resonant currents cross zero at the exact MOSFETs' switching points, indicating the peak-gain point operation; the average output currents are exactly 50 A. These simulation results demonstrate the accuracy of the proposed design algorithm—the design candidates have the exact peak gain at the exact minimum switching frequency.

B. Component Stress Comparison

The design results with the exact peak gain are listed in Table II. A component stress comparison is necessary to reveal the performance differences of the candidate designs. Design Nos. 1, 10, 20, and 25 are selected to perform the study using a simulation approach.

Table III summarizes component stresses of above design candidates at nominal input voltage and 50% load, which is selected as the optimization point of this design example. It can be observed that, as the Design No. increases from 1 to 25, both the L_r and the L_p's RMS current and flux swings decrease; the peak C_r voltage decreases as well; the secondary-side RMS

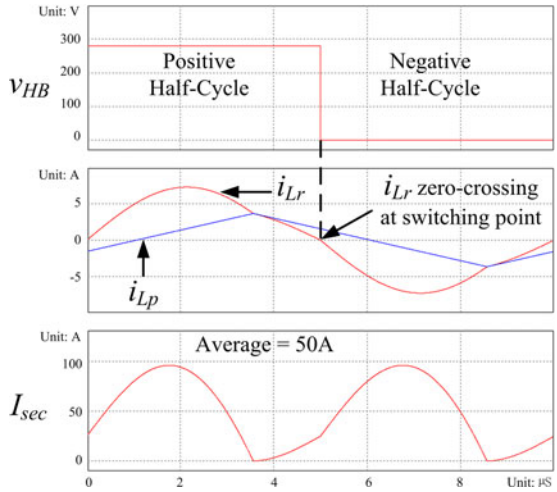

Fig. 2. Peak-gain point of Design Example 1. Design No. 10. $V_{\rm in} = 280$ V, $V_o = 12$ V, $F_s = 100$ kHz. Output current is exactly 50 A.

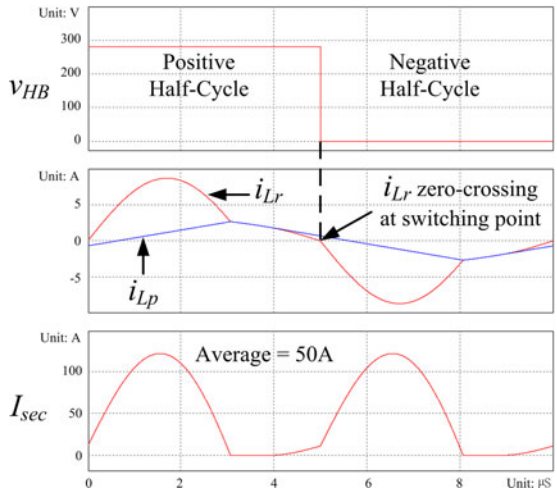

Fig. 3. Peak-gain point of Design Example 1. Design No. 20. $V_{\rm in} = 280$ V, $V_o = 12$ V, $F_s = 100$ kHz. Output current is exactly 50 A.

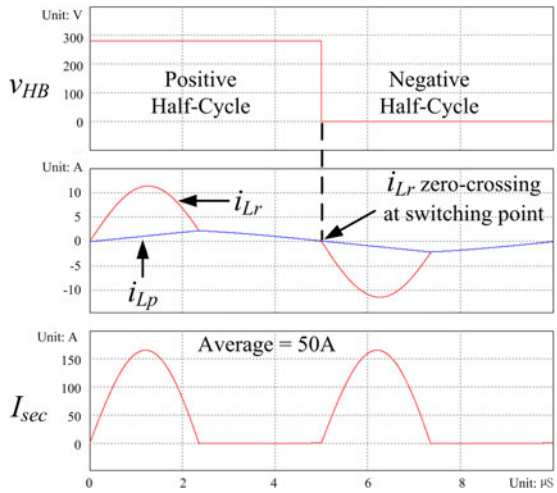

Fig. 4. Peak-gain point of Design Example 1. Design No. 25. $V_{\rm in} = 280$ V, $V_o = 12$ V, $F_s = 100$ kHz. Output current is exactly 50 A.

TABLE III
COMPONENT STRESSES OF DESIGN EXAMPLE 1 (NOMINAL INPUT VOLTAGE AND 50% LOAD)

Design No.	RMS secondary current	RMS L_r current	Peak L_r current	Peak L_r flux	RMS L_p current	Peak L_p current	Peak L_p flux	Peak C_r voltage
1	29.5 A	3.4 A	4.9 A	1.867 mWb	2.4 A	4.1 A	0.458 mWb	1436 V
10	28.8 A	2.8 A	4.1 A	0.507 mWb	1.8 A	3.1 A	0.407 mWb	559 V
20	28.2 A	2.2 A	3.1 A	0.146 mWb	1.1 A	1.9 A	0.339 mWb	329 V
25	28 A	2 A	2.9 A	0.062 mWb	0.7 A	1.3 A	0.258 mWb	267 V

TABLE IV
COMPONENT STRESSES OF DESIGN EXAMPLE 1 (MINIMUM INPUT VOLTAGE AND FULL LOAD)

Design No.	RMS secondary current	RMS L_r current	Peak L_r current	Peak L_r flux	RMS L_p current	Peak L_p current	Peak L_p flux	Peak C_r voltage
1	57.7 A	4.8 A	6.9 A	2.628 mWb	2.5 A	4.3 A	0.480 mWb	1926 V
10	60.6 A	4.9 A	7.3 A	0.903 mWb	2.1 A	3.7 A	0.485 mWb	854 V
20	68.6 A	5.2 A	8.7 A	0.409 mWb	1.6 A	2.7 A	0.474 mWb	569 V
25	80.6 A	5.8 A	11.4 A	0.243 mWb	1.3 A	2.2 A	0.436 mWb	497 V

current is almost the same. These trends show that the designs with larger Design No. (or higher resonant capacitor value) have lower RMS current and magnetic flux swing at the optimization point (nominal input voltage, 50% load), thus have lower total loss. The reduced RMS current is mainly due to the increased L_p value which decreases the primary-side circulating current.

Table IV summarizes component stresses of above design candidates at minimum input voltage and full load, which is usually the worst-case point. It can be observed that, as the Design No. increases (or resonant capacitance increases), the RMS secondary-side current will increase, which has the most significant impact on efficiency; the L_r current stress increases slightly but flux swing significantly decreases; the L_p current stress decreases but the flux swing is almost identical; the C_r voltage stress decreases. Above observations show that 1) the same transformer core can be used for all of these designs because the transformer flux swings are the same; 2) designs with larger resonant capacitor value possibly have lower efficiency at the worst-case point due to the increased RMS secondary current, but the resonant inductor can be made smaller due to the reduced flux swing.

In conclusion, above comparisons show that the largest Design No. candidate (No. 25 in this example, or the largest resonant capacitor value) has the lowest component stress at the optimization point (the unity-gain point), and possibly uses the smallest physical resonant inductor, but sacrifices the worst-case efficiency (in the below-resonance region) due to the increased RMS secondary current. If the design objective is to optimize efficiency at the unity-gain point, the largest Design No. candidate (larger resonant capacitor value) should be selected. However, since the largest Design No. candidate also has the largest L_p value, the ZVS condition must be verified. In addition, if an LLC converter is expected to operation at below-resonant frequency for extended periods, selecting a smaller L_p value design will result in a higher overall efficiency.

C. ZVS Consideration

The proposed design algorithm is derived based on the peak-gain requirement, but does not consider the ZVS requirement. This is because the dead time can be defined according to the resonant current at the MOSFETs' turn-off point. As a general thought, the dead time can be as long as needed to achieve ZVS. However, depending on the applications, there are two scenarios.

1) Peak-Gain-Dominated Designs: This scenario happens in high-power and/or high-gain applications. The L_p value must be sufficiently small to provide the required peak gain, such that all of the candidate designs can provide the ZVS condition. A design example is provided further below in this section.

2) ZVS-Dominated Designs: In this scenario, the design candidate with the largest L_p value cannot achieve ZVS even with the longest possible dead time. Therefore, a design candidate with a smaller L_p value should be selected. A detailed explanation is below.

The analysis in Section II-B2 shows that design candidates with large L_p values are preferred because they feature lower RMS current stress, and, thus, higher efficiency at the optimization point. However, large L_p values also result in small turn-off current, and, thus, require long dead time to achieve ZVS, but the maximum dead time length is limited by the resonant current's zero-crossing point; the resonant current's phase angle reduces with the increase of output voltage gain and load current; if the dead time interval is extended to the current zero-crossing point, the ZVS condition is lost. As a result, in a ZVS-dominated design, the L_p value, and the dead time length must have tradeoff to provide ZVS for the required operation range.

Continuing the above design example, simulation results suggest that the Design No. 25 (with 30-nF resonant capacitance) cannot provide ZVS at 375-V input voltage/full load. According to the above discussion, this is a ZVS-dominated design. After examining Design Nos. 24, 23, and 22, consecutively, simulation results show that Design No. 22 (with 27-nF resonant capacitance) can provide ZVS at 375-V input voltage using 550-ns dead time. This design has the largest L_p value and meets the ZVS requirement. Therefore, it will provide the best efficiency at nominal input voltage compared to other design candidates in Table II. The simulation waveforms to demonstrate the ZVS condition are shown in Fig. 5.

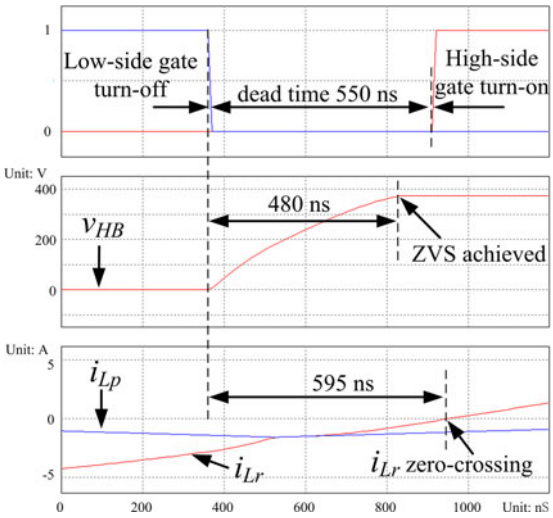

Fig. 5. ZVS condition for Design No. 22. $V_{\rm in} = 375$ V, $V_o = 12$ V, $P_o = 600$ W, $C_j = 1$ nF.

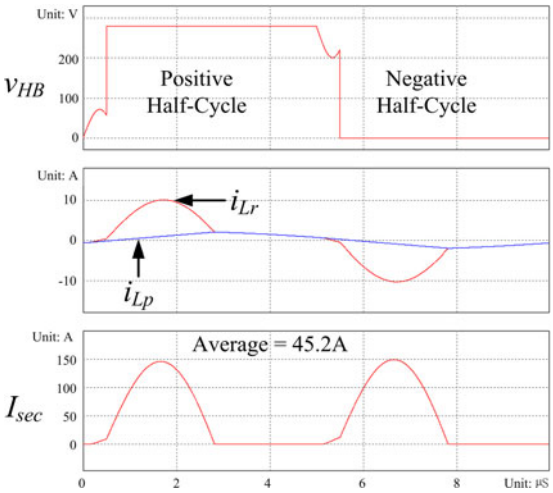

Fig. 6. Peak-gain point for Design No. 25. $V_{\rm in} = 280$ V, $V_o = 12$ V, $F_s = 100$ kHz, $C_j = 1$ nF, $t_d = 500$ ns. Output current is reduced to 45.2 A.

D. Peak-Gain Reduction by Dead Time

The dead time interval is usually ignored in the analysis because it is short compared to the switching period. However, the charging/discharging of MOSFETs' junction capacitance slightly changes the resonant tank's trajectory and has an effect to reduce the output voltage gain. In normal operation, this gain reduction is compensated by operating at a slightly lower switching frequency, but at the peak-gain point, the switching frequency cannot be reduced anymore; thus, the peak voltage gain will be lower than the designed value. In addition, at the peak-gain point, the resonant current reverses direction during the dead time interval; thus, the high-side MOSFET will block input current for a time period, further reducing the output power. An example is shown in Fig. 6, where the Design No. 25 with 500-ns dead time can only provide 45.2-A load current instead of 50-A as shown in Fig. 4.

Two methods can be used to solve this problem: 1) design margin, and 2) adaptive dead time.

TABLE V
SPECIFICATION OF DESIGN EXAMPLE 2

Nominal input voltage	400 V
Minimum input voltage	350 V
Minimum input voltage with ZVS	375 V
Maximum Output voltage	56 V
Minimum switching frequency	100 kHz
Full load power	2.4 kW
Transformer turns ratio	16:4

TABLE VI
DESIGN RESULTS OF DESIGN EXAMPLE 2

Design No.	C_r (nF)	L_r (μH)	L_p (μH)	Resonant Frequency (kHz)
1	16	144.5232	44.7401	104.6626
5	20	112.6691	45.7016	106.0236
10	25	87.0766	47.0483	107.8697
15	30	69.8971	48.5933	109.9082
20	35	57.5052	50.3917	112.1844
25	40	48.0829	52.5234	114.7611
30	45	40.6127	55.1096	117.7289
35	50	34.4737	58.3460	121.2248

Leaving some design margin to compensate for the peak-gain reduction is very convenient; however, it will compromise the peak efficiency to some degree.

Adaptive dead time control is also convenient with digital controllers. At near the peak-gain point, the dead time should be reduced to minimum—just long enough to avoid shoot through. Losing ZVS is not a concern in this scenario, because it is not achievable near the peak-gain point anyway. Nevertheless, ZCS can be achieved if the MOSFET is turned ON near the resonant current zero-crossing point.

E. Design Example 2: Peak-Gain-Dominated Design

As discussed in Section II-C, in high-power and/or high-gain applications, the design results are dominated by the peak-gain requirement, and they all provide ZVS. This section provides such an example.

The design specification for a telecom application is summarized in Table V. The design results from the proposed algorithm are in Table VI. The main difference of Design Example 2 and Design Example 1 is that the output power is increased from 600 to 2400 W with output voltage of 56 V.

The ZVS requirement is not a limiting factor in this design example, because the design result with the largest L_p value (Design No. 35) can easily meet the ZVS requirement. The ZVS waveforms are shown in Fig. 7.

It is noted that, in this example, the nominal operating condition ($V_o = 56$ V) is not at the unity-gain point ($V_o = 50$ V). Therefore, the LLC converter should be optimized for below-resonance operation. According to the discussion in Section II-B, the design with the largest L_p has the largest secondary RMS current in the below-resonance region. Hence, the optimal design may not be the Design No. 35 but a design with a slightly smaller L_p value. The design decision should be made based on the component stress study.

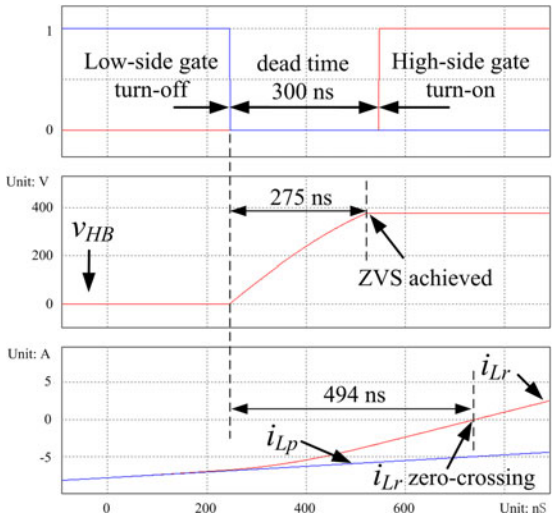

Fig. 7. ZVS condition for Design No. 35. $V_{\rm in} = 375$ V, $V_o = 56$ V, $P_o = 2.4$ kW, $C_j = 2$ nF.

F. Component Tolerance Consideration

The design results in above design examples are given to four decimal places. This is exaggerated but necessary to demonstrate the accuracy of the proposed algorithm. In practice, the component values have tolerances and can never be that accurate. However, the accurate design results draw a boundary of the theoretical limit. The designers can rely on it and add design margins as they feel comfortable. The following observations will be helpful when component tolerances are taken into consideration.

1) Deviated from the accurate design results, reducing L_p value will provide higher peak gain.
2) Deviated from the accurate design results, reducing L_r value and increasing C_r value will provide higher peak gain.
3) Since the accurate design results critically meet the peak-gain requirement, when consider component tolerances, the maximum possible inductor values must be smaller than the accurate design results, and the minimum possible resonant capacitor value must be greater than the accurate design result.
4) When loss is take into consideration, the full-load current used in the design algorithm should be the required full-load current divided by the worst-case efficiency.

III. Design of LLC Converter at Arbitrary Resonant Frequency

The proposed design algorithm so far only provides design solutions that achieve the same peak gain at the same minimum switching frequency. The resonant frequencies are different, which means the switching frequencies at nominal operating conditions cannot be specified by the designer. It is recognized that some designers prefer specifying the resonant frequency instead of the minimum switching frequency. In this section, characteristics of the design results are explored, and the design results can be used to design an LLC converter with a specified resonant frequency.

A. Characteristic Impedance and Turn-Off Current

Using the same design specification in Table I, but execute the proposed design algorithm with 100-, 200-, 400-, and 800-kHz minimum switching frequency, the design results are shown in Tables VII–X, respectively. In each table, the characteristic impedance of each design is calculated using (1), and the turn-off current at the resonant frequency is estimated using (2). The inductance ratio is defined as L_p/L_r

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \tag{1}$$

$$I_{\rm turn-off} = \frac{N \cdot V_o}{4L_p \cdot F_r}. \tag{2}$$

In Tables VII–X, there are fewer design results in higher frequency ranges. This is because the design algorithm takes 1 nF as incremental step for C_r to search for potential designs. In higher frequency ranges, several design solutions may be concentrated within a 1 nF incremental step, thus are omitted by the algorithm. Since high-voltage rating film capacitors start from 1 nF, it is not necessary to have finer incremental step for C_r.

When comparing Tables VII–X, it is observed that although the frequency ranges of these designs are very different, if we look at the characteristic impedance, the inductance ratio, and the turn-off current, the same values in one table (highlighted by shade) appear again in the next table

Above observation suggests that, LLC resonant tanks can be characterized by the characteristic impedance and the turn-off current (or the inductance ratio), and are irrelevant to the resonant frequency. This is not a surprising observation, as an equivalent insight has been observed in [32], [38], and [42], that an LLC resonant tank can be characterized by quality factor and inductance ratio. Here, characteristic impedance and quality factor are equivalent by their definitions; inductance ratio and turn-off current are equivalent as proved below. From (1), (2), and the definitions of K (inductance ratio) and F_r (resonant frequency), it can be derived that

$$I_{\rm turn-off} = \frac{N \cdot V_o \cdot \pi}{2K \cdot Z_0}. \tag{3}$$

Therefore, the turn-off current at resonant frequency can be expressed by a function of inductance ratio, thus they are equivalent variables to define an LLC design. Using turn-off current instead of inductance ratio to characterize an LLC resonant tank is better, because it intuitively suggests the ZVS condition at resonant frequency.

As a result, the design solution at one resonant frequency can be easily transformed into another design at an arbitrary resonant frequency by keeping the characteristic impedance and the turn-off current the same. The two designs will have the same peak gain value.

The transformation can take place using the following equations, where Z_0 and $I_{\rm turn-off}$ are calculated from the existing design result using (1) and (2), F_r is the desired resonant

TABLE VII
DESIGN RESULTS OF DESIGN EXAMPLE 1 WITH 100-KHZ MINIMUM SWITCHING FREQUENCY

Design No.	C_r (nF)	L_r (μH)	L_p (μH)	Resonant Frequency (kHz)	Characteristic Impedance (Ω)	Inductance Ratio	Turn-off Current at Fr (A)
1	6	380.9244	111.7068	105.275	251.967	0.293	4.082
3	8	274.6931	114.9072	107.3622	185.301	0.418	3.891
5	10	210.597	118.6049	109.6716	145.120	0.563	3.690
7	12	167.5096	122.9453	112.256	118.149	0.734	3.478
9	14	136.3598	128.1435	115.1895	98.691	0.940	3.252
11	16	112.5902	134.5183	118.5796	83.886	1.195	3.009
13	18	93.6432	141.9404	122.5874	72.128	1.516	2.759
15	20	77.9608	150.3098	127.458	62.434	1.928	2.505
17	22	64.5188	159.7177	133.5875	54.154	2.476	2.250
19	24	52.5925	170.1615	141.6617	46.812	3.235	1.991
21	26	41.6328	181.3471	152.9733	40.016	4.356	1.730
23	28	31.2196	192.1061	170.2266	33.391	6.153	1.468
25	30	21.2914	198.3318	199.1394	26.640	9.315	1.215

TABLE IIIV
DESIGN RESULTS OF DESIGN EXAMPLE 1 WITH 200-KHZ MINIMUM SWITCHING FREQUENCY

Design No.	***C_r(nF)***	***L_r(μH)***	***L_p(μH)***	***Resonant Frequency (kHz)***	***Characteristic Impedance (Ω)***	***Inductance Ratio***	***Turn-off Current at Fr (A)***
1	3	190.4622	55.8534	210.5499	251.967	0.293	4.082
2	4	137.3466	57.4536	214.7243	185.302	0.418	3.891
3	5	105.2985	59.3024	219.3431	145.120	0.563	3.690
4	6	83.7548	61.4727	224.512	118.149	0.734	3.478
5	7	68.1799	64.0717	230.379	98.691	0.940	3.252
6	8	56.2951	67.2591	237.1592	83.886	1.195	3.009
7	9	46.8216	70.9702	245.1748	72.128	1.516	2.759
8	10	38.9804	75.1549	254.916	62.434	1.928	2.505
9	11	32.2594	79.8589	267.175	54.154	2.476	2.250
10	12	26.2963	85.0808	283.3235	46.812	3.235	1.991
11	13	20.8164	90.6736	305.9467	40.016	4.356	1.730
12	14	15.6098	96.0531	340.4532	33.391	6.153	1.468
13	15	10.6457	99.1659	398.2789	26.640	9.315	1.215

TABLE IX
DESIGN RESULTS OF DESIGN EXAMPLE 1 WITH 400-KHZ MINIMUM SWITCHING FREQUENCY

Design No.	***C_r(nF)***	***L_r(μH)***	***L_p(μH)***	***Resonant Frequency (kHz)***	***Characteristic Impedance (Ω)***	***Inductance Ratio***	***Turn-off Current at Fr (A)***
1	2	68.6733	28.7268	429.4487	185.302	0.418	3.891
2	3	41.8774	30.7363	449.0241	118.149	0.734	3.478
3	4	28.1475	33.6296	474.3183	83.886	1.195	3.009
4	5	19.4902	37.5775	509.8319	62.434	1.928	2.505
5	6	13.1481	42.5404	566.647	46.812	3.235	1.991
6	7	7.8049	48.0265	680.9064	33.391	6.153	1.468

TABLE X
DESIGN RESULTS OF DESIGN EXAMPLE 1 WITH 800-KHZ MINIMUM SWITCHING FREQUENCY

Design No.	C_r (nF)	L_r (μH)	L_p (μH)	Resonant Frequency (kHz)	Characteristic Impedance (Ω)	Inductance Ratio	Turn-off Current at Fr (A)
1	1	34.337	14.363	858.8973	185.302	0.418	3.891
2	2	14.074	16.815	948.6366	83.887	1.195	3.009
3	3	6.574	21.27	1133.2994	46.812	3.235	1.991

TABLE XI
ORIGINAL DESIGNS IN TABLE II AND TRANSFORMED DESIGNS

	Original Designs Min. Fs = 100 kHz				Transformed Designs Fr = 500 kHz			
Design No.	C_r (nF)	L_r (μH)	L_p (μH)	Resonant Frequency (kHz)	C_r (nF)	L_r (μH)	L_p (μH)	Resonant Frequency (kHz)
1	6	380.9244	111.7068	105.275	1.2633	80.2036	23.5199	500
10	15	123.7436	131.1616	116.8189	3.5046	28.9112	30.6443	500
20	25	47.0212	175.7023	146.7923	7.3396	13.8047	51.5835	500
25	30	21.2914	198.3318	199.1394	11.9484	8.4799	78.9914	500

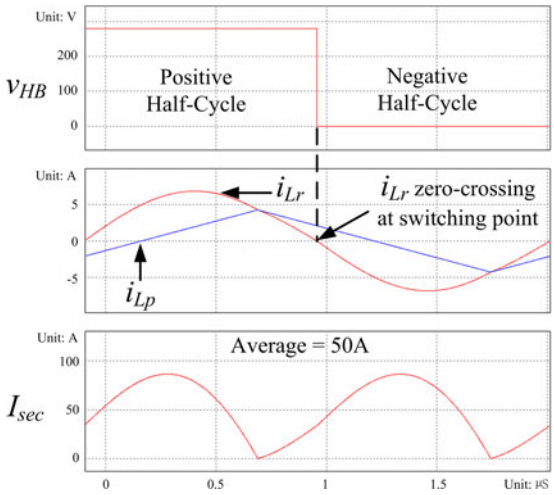

Fig. 8. Peak-gain point of Design Example 3. Design No. 1. $V_{\rm in} = 280$ V, $V_o = 12$ V, $F_s = 474.9$ kHz. Output current is exactly 50 A.

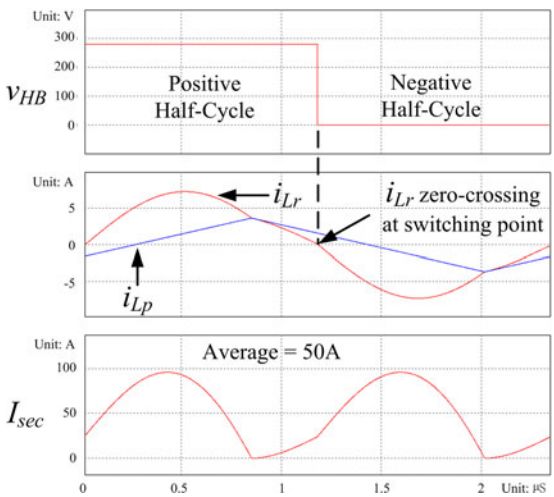

Fig. 9. Peak-gain point of Design Example 3. Design No. 10. $V_{\rm in} = 280$ V, $V_o = 12$ V, $F_s = 429$ kHz. Output current is exactly 50 A.

frequency, L_p, L_r, C_r, are the transformed new design

$$L_r = \frac{Z_0}{2\pi F_r} \tag{4}$$

$$C_r = \frac{1}{4F_r^2\pi^2 L_r} \tag{5}$$

$$L_p = \frac{N \cdot V_o}{4I_{\rm turn-off} \cdot F_r}. \tag{6}$$

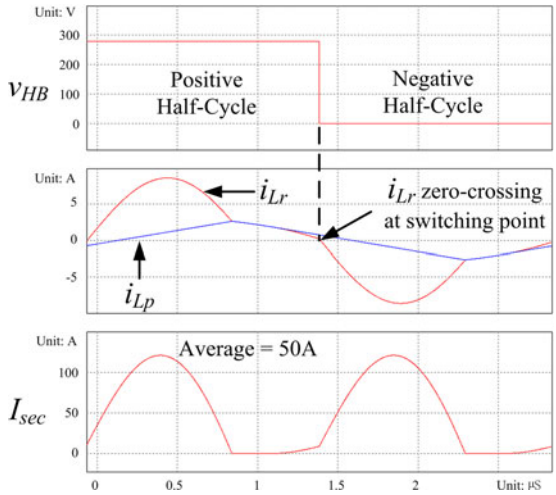

Fig. 10. Peak-gain point of Design Example 3. Design No. 20. $V_{\rm in} = 280$ V, $V_o = 12$ V, $F_s = 344$ kHz. Output current is exactly 50 A.

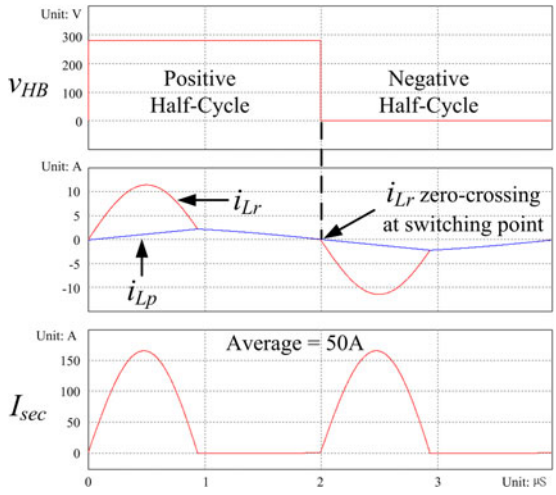

Fig. 11. Peak-gain point of Design Example 3. Design No. 25. $V_{\rm in} = 280$ V, $V_o = 12$ V, $F_s = 251$ kHz. Output current is exactly 50 A.

The above-described relation enables the proposed algorithm to design LLC converters with an arbitrary resonant frequency. It is also convenient for designers who wish to make decisions based on the turn-off current.

B. Design Example 3: Frequency Transformation

Using the same design specification in Table I, except specifying the resonant frequency at 500 kHz instead of specifying the minimum switching frequency. One can utilize (4)–(6) to transform the design results in Table II to new designs with

TABLE XII
COMPONENT STRESSES OF DESIGN EXAMPLE 3 (NOMINAL INPUT VOLTAGE AND 50% LOAD)

Design No.	RMS secondary current	RMS L_r current	Peak L_r current	Peak L_r flux	RMS L_p current	Peak L_p current	Peak L_p flux	Peak C_r voltage
1	29.5 A	3.4 A	4.9 A	0.323 mWb	2.4 A	4.1 A	0.096 mWb	1411 V
10	28.7 A	2.8 A	4 A	0.116 mWb	1.8 A	3.1 A	0.095 mWb	560 V
20	28.1 A	2.2 A	3.1 A	0.043 mWb	1.1 A	1.9 A	0.098 mWb	327 V
25	28.2 A	2 A	2.8 A	0.024 mWb	0.7 A	1.3 A	0.103 mWb	268 V

TABLE XIII
COMPONENT STRESSES OF DESIGN EXAMPLE 3 (MINIMUM INPUT VOLTAGE AND FULL LOAD)

Design No.	RMS secondary current	RMS L_r current	Peak L_r current	Peak L_r flux	RMS L_p current	Peak L_p current	Peak L_p flux	Peak C_r voltage
1	57.7 A	4.8 A	6.9 A	0.553 mWb	2.5 A	4.3 A	0.101 mWb	1926 V
10	60.6 A	4.9 A	7.3 A	0.211 mWb	2.1 A	3.7 A	0.113 mWb	853 V
20	68.7 A	5.2 A	8.6 A	0.119 mWb	1.6 A	2.6 A	0.134 mWb	565 V
25	80.6 A	5.8 A	11.5 A	0.098 mWb	1.3 A	2.2 A	0.174 mWb	497 V

TABLE XIV
SPECIFICATION OF DESIGN EXAMPLE 4

Nominal input voltage	400 V
Minimum input voltage	350 V
Output voltage	20 V
Resonant frequency	100 kHz
Full load power	65 W
Transformer turns ratio	10:1

TABLE XV
DESIGN RESULTS OF DESIGN EXAMPLE 4 ASSUME MINIMUM SWITCHING FREQUENCY IS 100 KHZ

Design No.	C_r (nF)	L_r (μH)	L_p (μH)	Resonant Frequency (kHz)	Characteristic Impedance (Ω)	Turn-off Current at Fr (A)
1	1	2264.61	1456.438	105.76	1504.862	0.325
2	2	952.709	1804.043	115.30	690.185	0.240

500-kHz resonant frequency. Four selected design results are shown in Table XI.

Figs. 8–11 show simulated peak-gain point waveforms of the transformed designs in Table XI.

Comparing with the original designs' waveforms in Figs. 1–4, the transformed designs have the same waveforms and load current, except different switching frequency. It is also observed that the normalized minimum switching frequencies of the original designs and the transformed designs are the same.

Tables XII and XIII summarize component stresses of the transformed designs in Table XI, at the optimization point (nominal input voltage and 50% load) and the worst-case point (minimum input voltage and full load), respectively. Comparing to the component stresses of the Design Example 1 in Tables III and IV, the transformed designs have the same RMS current and resonant capacitor voltage; the flux swings are smaller due the increased switching frequency.

Above studies demonstrate that, if two LLC designs have the same characteristic impedance and the same turn-off current at their respective resonant frequencies, they will have the same component stresses.

C. Design Example 4: ZVS-Dominated Design (Extreme Case)

This section demonstrates an extreme case for low-power and low-peak-gain applications, where none of the design results can meet the ZVS requirement. A design example is provided below.

A laptop adapter's specification is summarized in Table XIV.

Taking into consideration the design margins, the full load power value used in the design algorithm is set to 90 W. The proposed design algorithm yields only two design results, listed in Table XV.

It is noticed that the turn-off current of both design results is too small to provide ZVS for MOSFETs (assuming $C_j > 1$ nF). This is because the output power and gain requirements in this application are very low, any design with greater turn-off current will result in overdesign in terms of peak gain, thus they are not identified by the algorithm. Nevertheless, the design results provide the theoretical boundary for the peak-gain requirement. Based on either of the two designs, any greater turn-off current or/and smaller characteristic impedance will have greater peak gain, and then the design decision can be based on other requirements (e.g., ZVS, capacitor voltage stress, practical value of leakage inductance, etc.).

Based on Design No. 1 in Table XV, without the loss of generality, the turn-off current can be chosen to be 2 A to meet the ZVS requirement; then, the corresponding solution at 100-kHz resonant frequency is calculated as

$$L_p = 250\ \mu\text{H}, \quad L_r = 2395\ \mu\text{H}, \quad C_r = 1.058\ \text{nF}. \tag{7}$$

The design in (7) is guaranteed to meet the peak gain and the ZVS requirements, but the resonant inductance is impractically large. Again, without the loss of generality, the L_r and C_r can be reduced/increased by 47.9 times and the corresponding result is

$$L_p = 250\ \mu\text{H}, \quad L_r = 50\ \mu\text{H}, \quad C_r = 50.7\ \text{nF}. \tag{8}$$

The design in (8) has further increased peak gain, because its characteristic impedance is lower than that in (7).

Above design example shows that, in low-power low-peak-gain applications, the peak-gain requirement is not a dominant factor; thus, the proposed algorithm tends to provide design results with very large characteristic impedance and very low turn-off current. The designers can be confident to increase the turn-off current and decrease the characteristic impedance in order to accommodate other requirements, because the peak gain will only be increased after making such changes.

IV. Design Flowchart

The design examples above show three possible application scenarios.

Case 1: The parallel inductance value is determined by peak-gain requirement. In this case, all the design candidates provided by the proposed algorithm can provide ZVS and eliminate overdesign. The optimal design exists among the candidates and depends on the optimization point(s).

Case 2: The parallel inductance value is determined by the ZVS requirement. In this case, all the design candidates provided by the proposed algorithm can only meet the peak-gain requirement but cannot provide ZVS. Designers can modify the design candidates for ZVS and be confident to know that they all meet or exceed the peak-gain requirement.

Case 3: Between Case 1 and Case 2, some design candidates can meet both peak gain and ZVS requirements, and some design candidates can only meet the peak-gain requirement. In this case, designers can carefully select MOSFET and verify that the resonant current angle is large enough to realize ZVS. There can be a tradeoff in MOSFET selection; larger MOSFETs have lower $R_{\mathrm{ds(on)}}$ but also larger C_j which require larger resonant current angle for ZVS. Larger resonant current angle means higher RMS current which offsets the benefit of low $R_{\mathrm{ds(on)}}$. The optimal design exists among the candidates and depends on the optimization point(s).

In all three scenarios, efficiency tradeoff in different operating conditions, MOSFET selection, dead time length, and other secondary considerations (e.g., no-load operation, short-circuit operation, soft-start inrush current, switching frequency variation range, etc.) can be considered in the last step by investigating a few design candidates. Hence, using the proposed algorithm and design methodology, the peak-gain problem, the ZVS problem, the efficiency tradeoff, and other design considerations are decoupled into separate design steps. The design process is straightforward. The iterations in decision making are minimized. In comparison, the conventional design methods mix all design requirements together, and are, therefore, complicated and incomprehensive in searching for an optimal design.

Based on above discussions, a flowchart is developed in Fig. 12 to help designers better utilize the proposed algorithm. The steps in the flowchart are explained as follows.

Step 1: Specification. The input parameters include minimum input voltage, output voltage, minimum load resistance, minimum switching frequency, and transformer turns ratio.

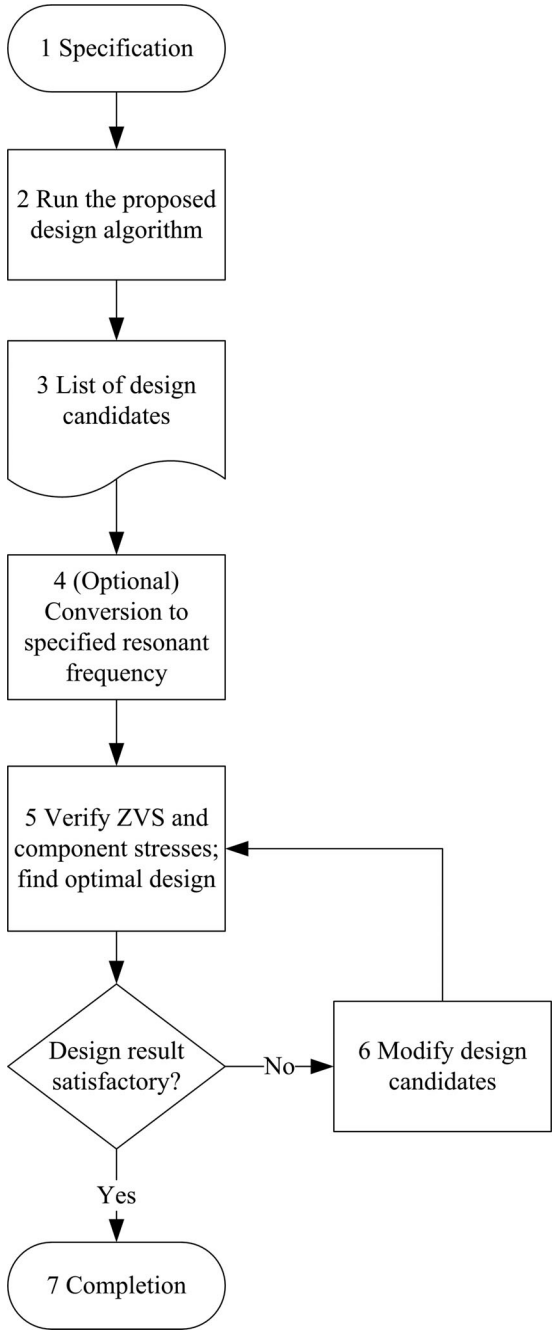

Fig. 12. Design flowchart.

The minimum switching frequency can be determined by considering the saturation limit of the selected core

$$B_{\mathrm{sat}} \cdot A_e \cdot N_p \geq \frac{V_o \cdot N}{f_{s,\min}} \Rightarrow f_{s,\min} \geq \frac{V_o \cdot N}{B_{\mathrm{sat}} \cdot A_e \cdot N_p} \quad (9)$$

where B_{sat} is the saturation limit of the selected material, A_e is the effective area of the selected core, N_p is the primary-side turns, and N is the turns ratio.

In the case, where the resonant frequency is specified, the minimum switching frequency can be selected as an arbitrary number in this step, as long as it yields sufficient design candidates. Usually a lower minimum switching frequency will yield more design candidates.

TABLE XVI
SPECIFICATION OF PROTOTYPE

Nominal input voltage	384 V
Minimum input voltage	300 V
Output voltage	12 V
Full load current	50 A
Transformer turns ratio	16 : 1
Resonant frequency	300 kHz

TABLE XVII
PROTOTYPE PARAMETERS

Magnetizing Inductance	110 μH
Series Inductance	10 μH
Series Capacitance	6.8 nF $\times$ 4
Half-bridge MOSFET	Infineon 65F6110
SR MOSFET	NXP PSMN1R2 $\times$ 3
Transformer Core Size and Material	PQ40/3C95

It is desirable to leave some design margin in the design specification in order to take into account component tolerances and peak-gain reduction caused by dead time. For example, the minimum input voltage can be slightly reduced to ensure a robust design.

Step 2: Run the LLC design program.

Step 3: Collect a list of design candidates from Step 2.

Step 4: (Optional) Conversion to specified resonant frequency. The frequency transform can be carried out by the following steps.

1) Use (1) and (2) to convert the list of design candidates into an intermediate form which are expressed by the characteristic impedance and the turn-off current.
2) Use (4) to (6) to convert the intermediate-form design candidates into the specified resonant frequency.

Step 5: Verify ZVS condition and component stresses, and find the optimal design solution.

This step requires the designer's engineering judgment. Simulation can be used as an evaluation tool.

In general, the design with the largest L_p value has the lowest RMS current at the resonant frequency but the highest RMS current at the peak-gain point (lowest input voltage and full load). The designer should evaluate design candidates at different operating conditions, and find a proper tradeoff for the targeted application.

Also, the designer should select MOSFET, verify the ZVS condition, and determine a proper dead time length. In general, the design with the largest L_p value has the lowest turnoff current for ZVS. If ZVS is not achievable with the longest possible dead time, the design with the next largest L_p value should be considered.

In addition, if adaptive dead time control is not used, the designer should also check that, with the selected dead time length, whether the design can provide sufficient output power at minimum input voltage, because long dead time can slightly reduce the peak gain.

Furthermore, if there are other secondary considerations, such as no-load operation, short-circuit operation, soft-start inrush current, switching frequency variation range, etc., they can be incorporated into this step.

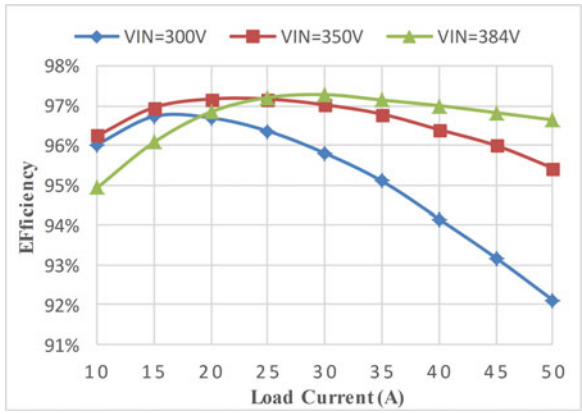

Fig. 13. Efficiency plot at $V_{\rm in} = 384$ V.

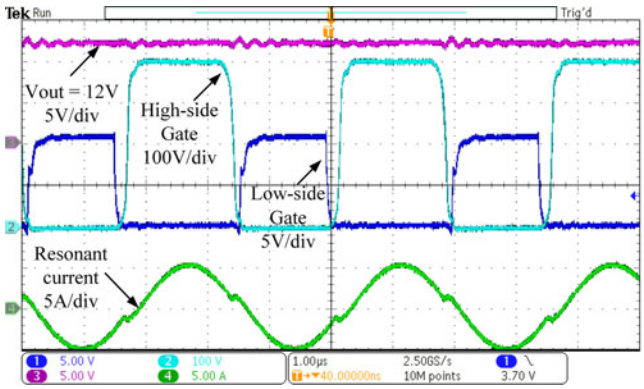

Fig. 14. Operation waveform at $V_{\rm in} = 384$ V, $I_o = 50$ A.

After the above evaluation, an optimal design can be identified. If the design result is satisfactory, the design procedure is completed. If no satisfactory design is found, enter Step 6.

Step 6: Modify design candidates. There are two possible reasons that no satisfactory design result is found: 1) ZVS is not achievable; 2) resonant capacitor voltage stress is too high. In both cases, the peak-gain requirement is no longer a limiting factor; thus, the design candidates from previous steps should be modified to meet other requirements. Reducing the L_p value can provide higher turn-off current. Reducing the characteristic impedance can reduce the resonant capacitor voltage stress. The related discussion is in Design Example 4.

Step 7: Design completion. Upon completion of the design, the actual available component values and component tolerances should be considered when selecting components. The discussion is in Section II-F.

V. EXPERIMENTAL RESULTS

A prototype is designed based on the specification in Table XVI and the design procedure proposed in Fig. 12. The design objective is to optimize efficiency at the nominal input voltage. The objective minimum input voltage is 300 V; 280 V is used in the design algorithm in order to leave some design

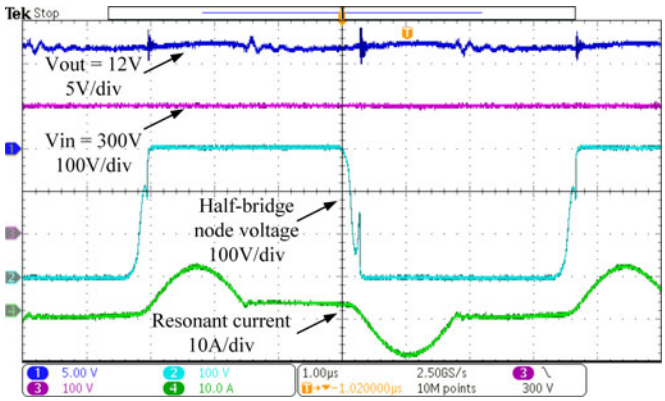

Fig. 15. Operation waveform at $V_{\rm in} = 300$ V, $I_o = 50$ A.

margin. After going through the design steps described in Section IV, the prototype parameters are determined and are shown in Table XVII.

The peak efficiency reached 97.3% at half load and 384-V input voltage. The efficiency plots of 300-, 350-, and 384-V input voltage conditions are shown in Fig. 13. The operation waveform at 384-V input voltage and 50-A load current is shown in Fig. 14. The operation waveform at 300-V input voltage and full load is shown in Fig. 15. In Fig. 15, the half-bridge node waveform shows the signs of loss of ZVS during dead time. This confirms the analysis in Section II-D.

VI. Conclusion

This paper proposed a new approach to find an optimal design for LLC converters. The core of the proposed method is an accurate design algorithm that can find all possible designs with the exact peak-gain value. Simulation results show that the proposed algorithm is very accurate. Through case studies, this paper demonstrated how to use the proposed algorithm in different application scenarios, and the considerations in design tradeoffs.

It is demonstrated that the candidate design with the largest parallel inductance features the lowest component stress at the resonant frequency but the highest component stress at the peak-gain point. Designers can identify among the candidates the optimal design for a particular application based on the loss analysis. Also, in low-power low-peak-gain applications, ZVS becomes the dominating requirement. Designers can modify the candidate designs by increasing the turn-off current and/or decreasing the characteristic impedance of the resonant tank in order to achieve ZVS, knowing that the peak-gain requirement will still be met.

Advantages of the proposed design algorithm include: 1) accuracy—it can eliminate overdesign of the peak-gain value, thus minimize component stresses; and 2) comprehensiveness and reduced design effort—it provides all possible designs that meet the peak-gain requirement in the first design step, such that designers can conveniently make tradeoffs according to individual applications.

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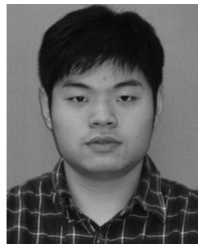

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